

FIG. 1

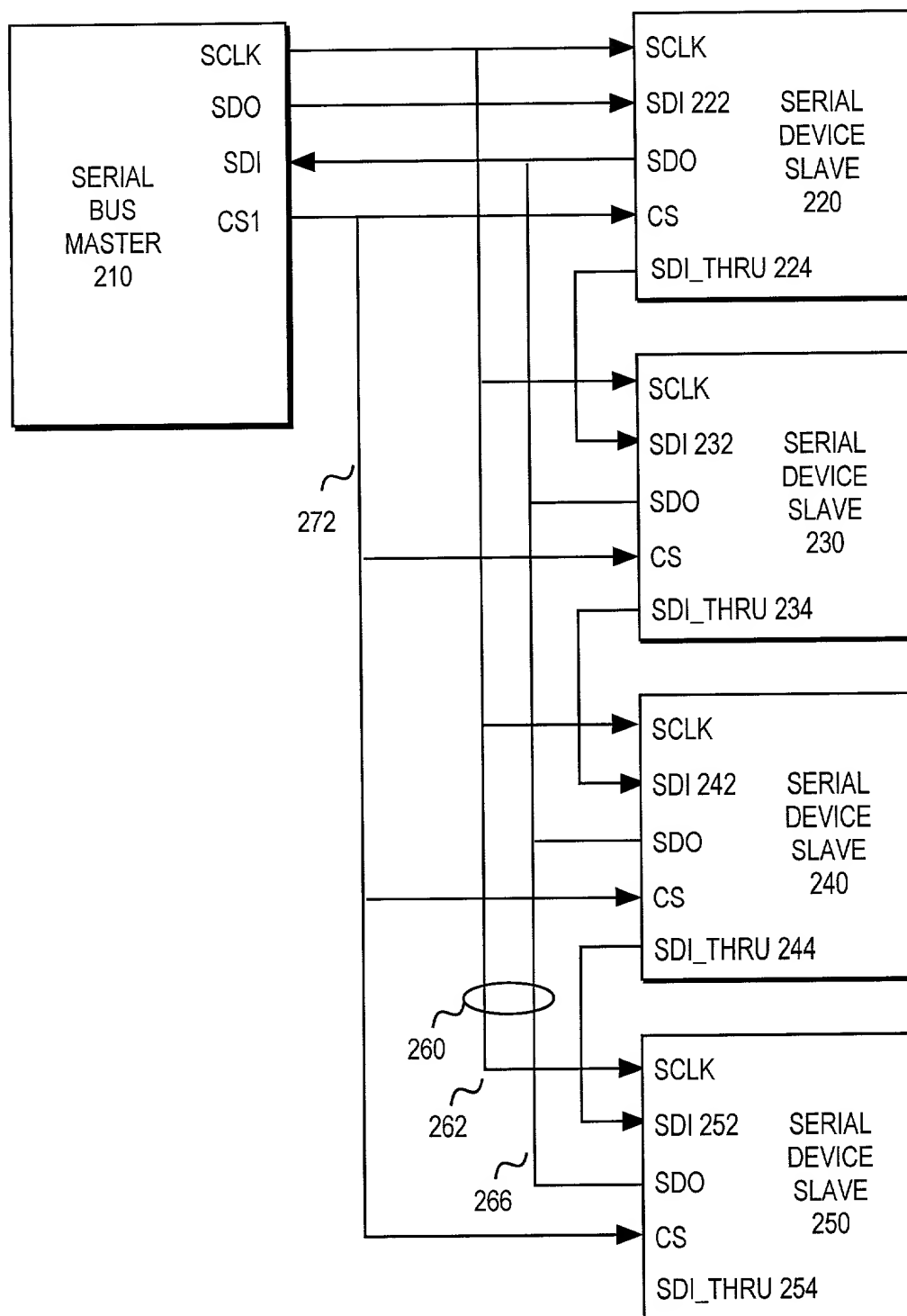


FIG. 2

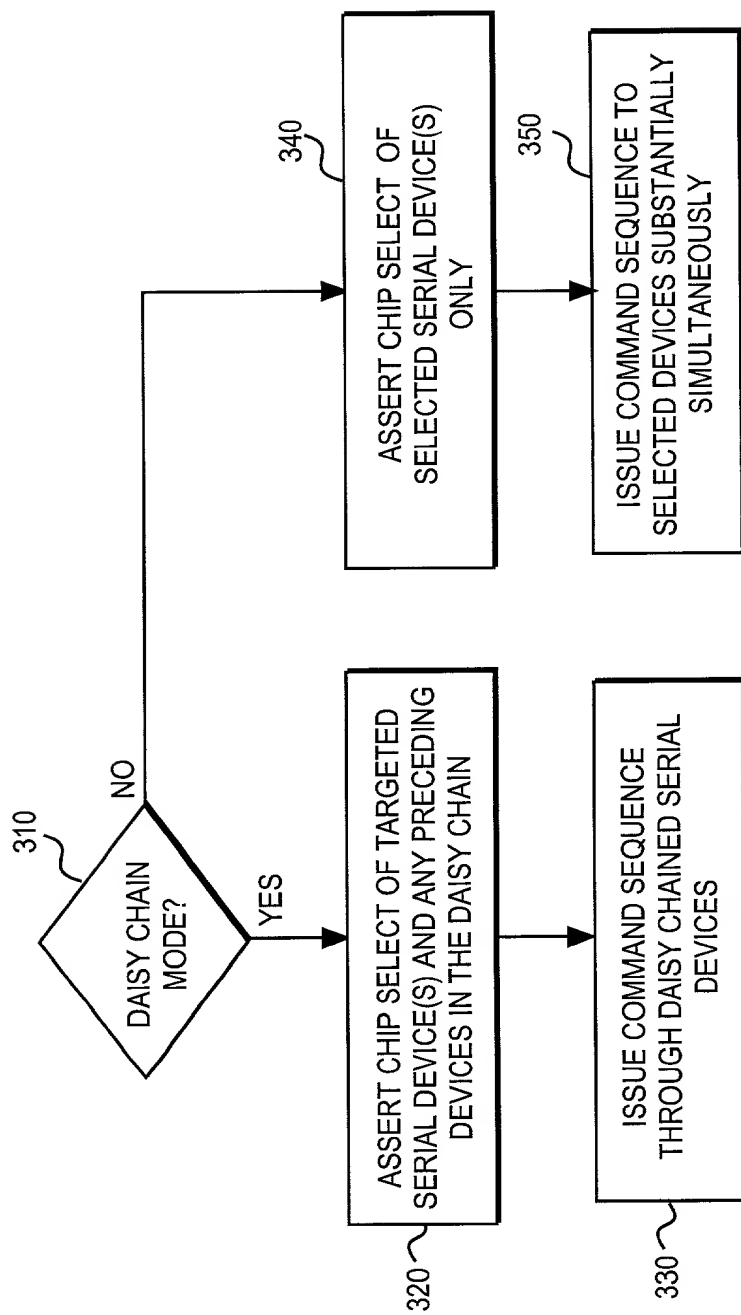


FIG. 3

FIG. 4 is a block diagram of a system 400 including a first device 400A and a second device 400N. The first device 400A includes a command sequence processing logic 420 and a command sequence execution logic 430. The second device 400N includes a command sequence processing logic 420 and a command sequence execution logic 430. The first device 400A is connected to the second device 400N via a serial data interface (SDI) 410 and a serial clock (SCLK) 412. The first device 400A also includes a serial data interface through (SDI_THRU) 432, which is connected to the second device 400N via a serial data interface (SDI) 410 and a serial clock (SCLK) 412.

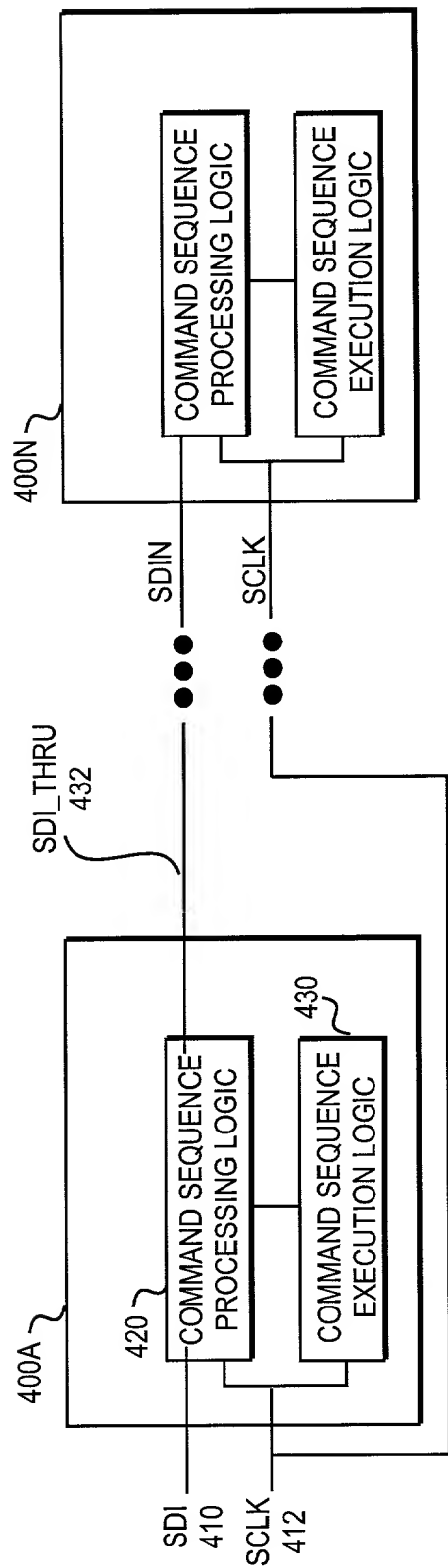


FIG. 4

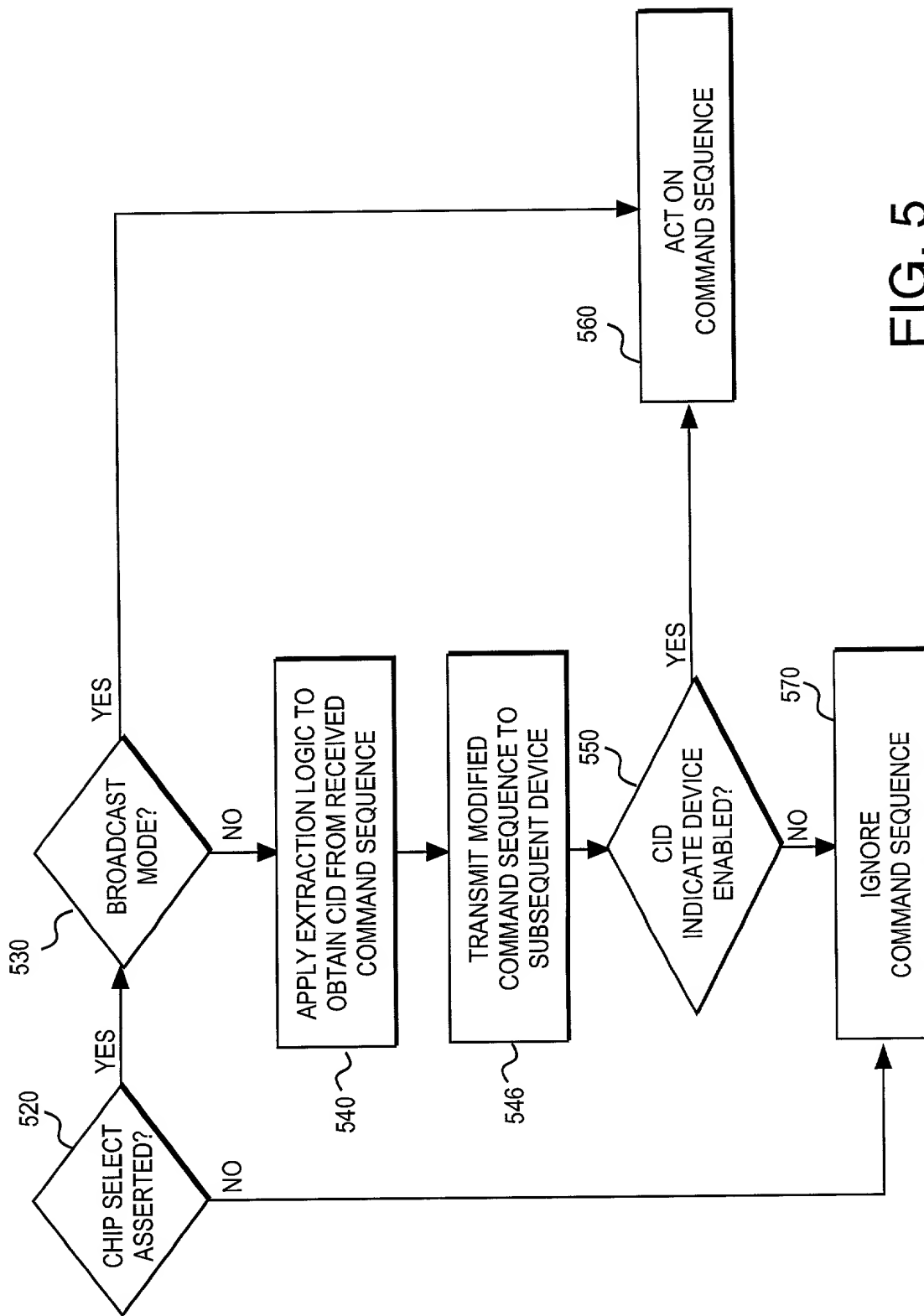


FIG. 5

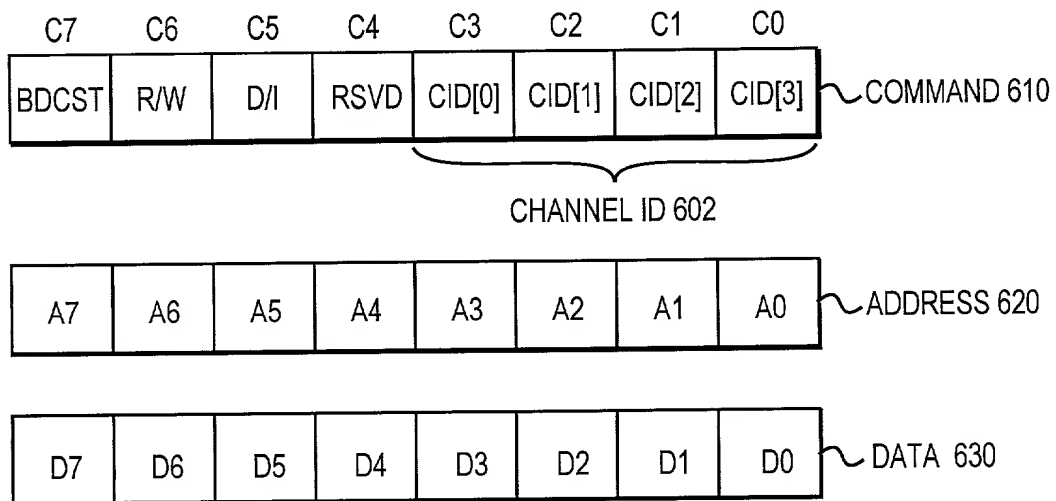
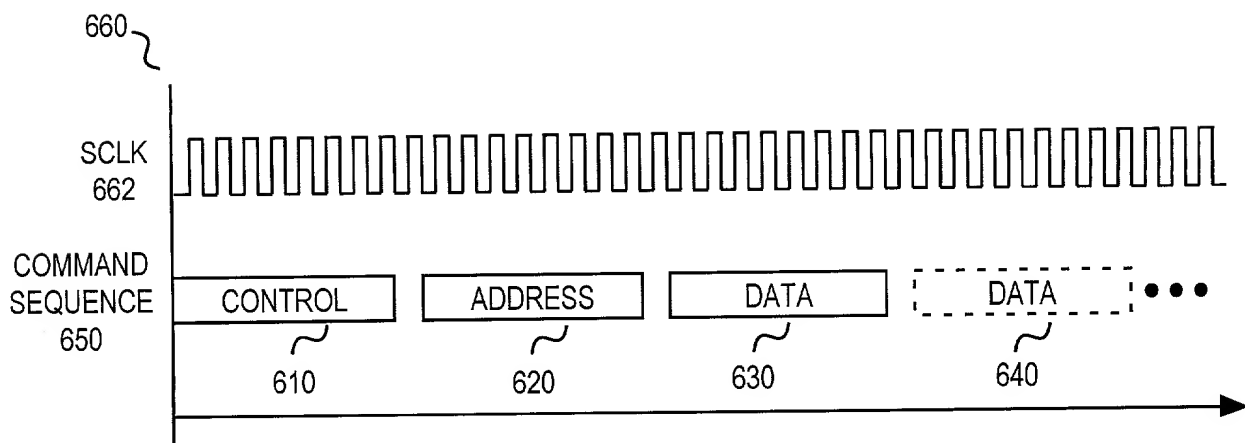


FIG. 6

<div>710 ~ TARGETED DEVICE</div>	<div>720 ~ EMBEDDED COMMAND WORD RECEIVED</div>	<div>730 ~ EMBEDDED COMMAND WORD TRANSMITTED</div>
0000	0000	1111
0001	1000	0000
0010	0100	1000
0011	1100	0100
0100	0010	1100
0101	1010	0010
0110	0110	1010
0111	1110	0110
1000	0001	1110
1001	1001	0001
1010	0101	1001
1011	1101	0101
1100	0011	1101
1101	1011	0011
1110	0111	1011
1111	1111	0111

FIG. 7

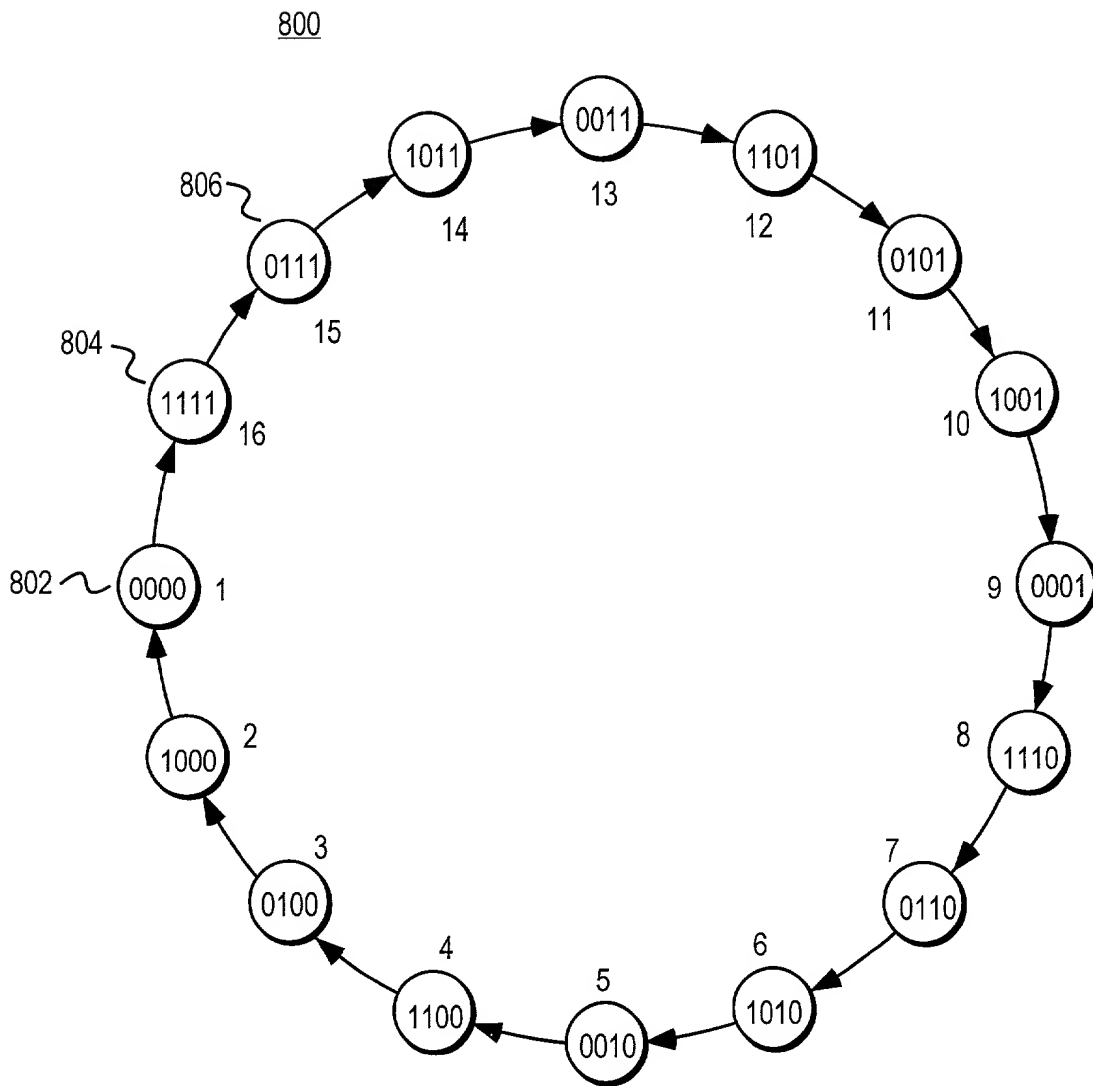


FIG. 8